University of Delaware
Newark, De 19716-3820
Ph: 302/831-6200
Fax: 302/831-6226
www.udel.edu/iec

INSTITUTE OF ENERGY CONVERSION

UNITED STATES DEPARTMENT OF ENERGY
UNIVERSITY CENTER OF EXCELLENCE
FOR PHOTOVOLTAIC RESEARCH AND EDUCATION

April 24, 2007

Bolko von Roedern
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

Re: NREL Subcontract #ADJ-1-30630-12
D.5.12

Dear Bolko,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of January 16, 2007 to February 15, 2007, under the subject subcontract. The report highlights progress and results obtained under Task 1 (CdTe-based solar cells).

Task 1 - CdTe-based Solar Cells

Summary

Issues related to high throughput processing of and junction-limiting factors in CdTe solar cells are reported. Based on the effects of TCO/substrate cleaning described in the previous report, we continued with the study of uncontrolled impurities originating in the glass/SnO_2 substrate. It is vital that this source of variability in film morphology and device performance is eliminated prior to development of cells with sub-micron absorber thickness and evaluation of approaches for V_{OC} > 900 mV. In this report, we present the details of procedures used to establish a performance baseline with cell efficiency >11% for processing CdTe/CdS cells with vapor transport deposited CdTe onto moving commercially available substrates at high growth rate (~10 µm/min) using rapid post-deposition processing, with less than 1 min per processing step.

Glass/TCO Preparation

Experiments were conducted to isolate the effects on CdTe films and devices of the actual cleaning of the as received glass/SnO_2 prior to any other processing steps. None of the samples were pre-baked prior to cleaning. A gallium oxide (Ga_2O_3) buffer layer was formed on all samples by 1) electrodeposition of 15–20 nm Ga (ED Ga) followed by 2) oxidation for 15 minutes at 550°C.

The method of cleaning and rinsing was varied to compare the length of time and type of solvent used for the wash, the purity of the water used for the rinse and the length of time and the temperature of the rinse (Table I). The solvent step was performed using our standard Crest cleaning system consisting of a 65°C ultrasonic soap (Liquinox) wash or a room temperature ultrasonic methanol/isopropyl alcohol wash for the times indicated. The De-ionized water rinse was performed in our standard Crest cleaning system ultrasonic tank. The hot Nanopure water rinse was performed in a large clean beaker held within the ultrasonic tank at ~70°C. For the 3 minute de-ionized water rinse, the temperature of the tank water typically drops from 85°C to 70°C during that time period. For the 10 minute de-ionized water rinse, the temperature was maintained at 80°C for the entire time. The water rinsed samples were dried in a forced hot air dryer while the methanol/isopropyl samples were dried with compressed argon gas. Following the oxidation step, all the samples received our baseline CdS and CdTe film deposition. Cells were processed with the established baseline vapor $CdCl_2$ treatment for 2 minutes at 480°C and aniline treatment, with Cu/Ni contacts.

Table I. Summary of cleaning and rinsing procedures used for 10 cm x 10 cm TEC15 plates.

Run Number	CdTe Thickness (μm)	ED Ga Dep Time (min)	Ga Oxidation Time (min)	Solvent	Rinse	Comments
240	5.3	20	80	Ultrasonic Liquinox 3 min	Ultra DI 3 min	Control
267	5.9	e-beam	75	Ultrasonic Liquinox 3 min	Ultra DI 3 min	
268	8.7	10	15	Ultrasonic Liquinox 3 min	Hot Ultra Beaker Nanopure 3 min	
269	5.9	10	15	Ultrasonic Liquinox 3 min	Hot Ultra Beaker Nanopure 3 min	New N_2 cylinder
270	6.6	12.5	15	Ultrasonic MeOH/IPA 10 min each	none	New O_2/N_2
271		12.5	15	Mix Liquinox/IPA	Mix Ultra DI/None	6 I"X1" Substrates
272	7.9	12.5	15	Ultrasonic Liquinox 3 min	Ultra DI 3 min	Vacuum Stored after Ga_2O_3
273	9.4	12.5	15	Ultrasonic Liquinox 3 min Ultrasonic Liquinox 10 min	Ultra DI 3 min Hot Ultra DI 10 min	Cleaned twice (first time 8/06)
274	6.3	12.5	15	Ultrasonic Liquinox 10 min	Hot Ultra DI 10 min	

Table II summarizes the device performance obtained after different cleaning and rinsing procedures of the TEC15 substrates. Focusing first on the short circuit current (J_{SC}), a *dramatic* loss in photocurrent is obtained for 2 cases: 1) with standard detergent cleaning but rinsing in a fixed volume of clean water in a beaker and 2) with a solvent-only clean (no water rinse). The JV and QE data for these low-J_{SC} cells is shown in Figures 1 and 2, respectively. The JV characteristics exhibit cross-over between the light and dark curves, with a soft diode and apparent voltage-dependent collection $J_L(V)$ effect. The QE, measured at 0V and at -1V, revealed only a weak dependence of collection with bias, with a constant ratio of the two measurements, suggestive of optical or interface loss. The correlation of this behavior with a low degree of rinsing strongly implicates electronic changes due to chemical contamination.

Table II. Best cell JV parameters for VT cells processed with different glass and window layer preparation.

Run Number	Glass/Window Clean and Ga deposition method	V_{OC} (mV)	J_{SC} mA/cm^2	FF (%)	Eff (%)
240.3	Control, ED Ga	782	24.8	68.8	13.3
267.3	Control, E-beam Ga	758	23.5	58.3	10.4
268.1	Beaker rinse, ED Ga	567	6.2	52.7	1.9
269.1	Beaker rinse, ED Ga	646	9.4	42.0	2.6
270.3	Solvent clean, ED Ga	666	2.1	49.9	0.8
272.1	Control, ED Ga	755	24.2	65.9	12.1
273.1	Long detergent step, ED Ga	707	18.8	55.7	7.4
274.1	Long detergent step, ED Ga	719	21.4	53.0	8.2

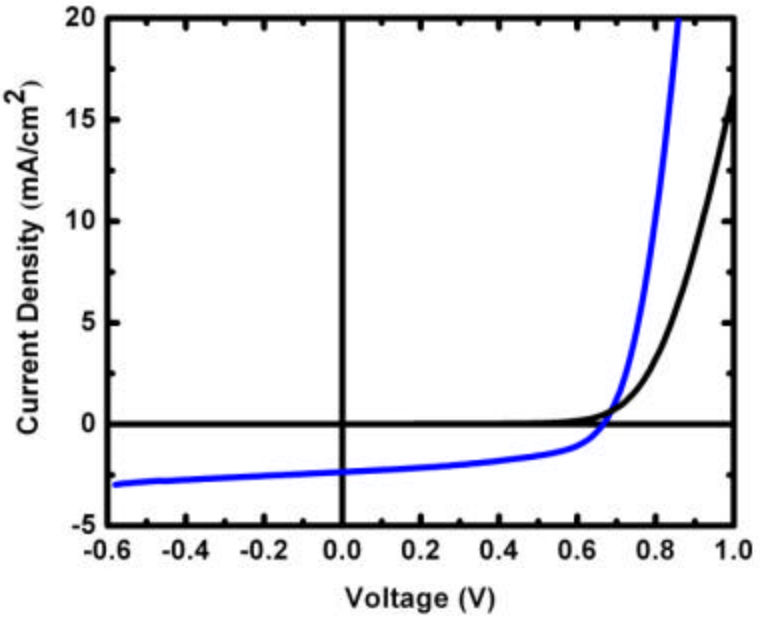


Figure 1. Light AM1.5 and dark JV characteristics of VT270, processed with solvent-only cleaning of the TEC15 superstrate glass/SnO_2 prior to ED Ga deposition.

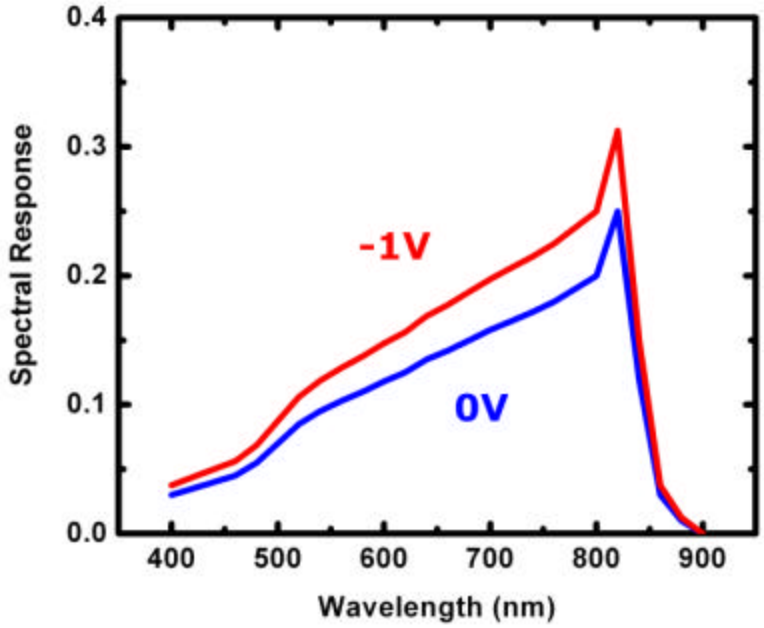


Figure 2. Dark QE at 0V and -1V of VT270, processed with solvent-only cleaning of the TEC15 superstrate glass/SnO_2 prior to ED Ga deposition.

Overall, the device results from Table II show that the most important glass handling step is the method of rinsing the glass after ultrasonic cleaning in Liquinox detergent, and that the detergent step is absolutely necessary for the TEC15 glass which has been cut by the supplier into 10 cm x 10 cm plates. The primary effect of insufficient rinsing in these samples is a loss in photocurrent and is likely due to low minority carrier lifetime, sufficient to kill transport through the film.

A further effort was initiated to examine the microscopic structural and compositional effects of different glass types, cleaning procedures and barrier layers on CdS film properties, with the goal of identifying the chemical agents responsible for reduced junction quality and transport. Issues such as oxide formation and impurity incursion into the CdS film will be examined for films deposited under different conditions onto different substrate/TCO/HR combinations. This will expand our understanding of the role of the buffer layer as both: 1) diffusion barrier against contaminants originating in different glass superstrates and 2) electrical component in the device that reduces lateral effects from low quality, i.e., high recombination, junctions.

High Throughput Processing

Over the past year, we have demonstrated the ability to maintain baseline cell performance for cells with CdTe films deposited at ~10 microns per minute onto a moving substrate using reduced post-deposition processing time. Vapor $CdCl_2$ processing time was reduced to 1 minute, while aniline etching was reduced to 2 minutes. During the present reporting period, experiments were conducted to further reduce processing time, to less than 1 minute for these two post-deposition treatments. Modification of the treatment protocol for reduced time was guided by our knowledge of the diffusion and oxidation processes in the CdTe/CdS thin film structures. The solid state diffusion which consumes CdS via CdTeS alloy formation is a critical aspect of processing, whereby V_{OC} is reduced when the CdS film is consumed sufficiently to create discontinuities; 3D modeling of the diffusivity of interstitial Cd through the polycrystalline film, the limiting process, taking into account the grain size distribution, allowed equivalent temperature-time configurations to be determined1. Furthermore, oxide formation on films processed at 350°Cto 500°C in air or in $CdCl_2$ vapor proceeds approximately linearly for times up to ~30 minutes, and the oxide composition and formation rate are both strong functions of the relative humidity of the ambient. Using GIXRD with *in-situ* heating plus atmospheric control and using XPS for *ex-situ* surface analysis, the oxidation rates, expressed as equivalent film accumulation rate, were determined for different temperatures and atmospheres (Table III).

Table III. Measured oxidation rate for CdTe film surface at 400°C.

Ambient P_T = 760 Torr $Ar/(Ar+O_2)$ = 0.80	Relative Humidity (%)	Crystalline Phases	Equiv film oxidation rate (nm/min)
$Ar + O_2$	<1	$CdTeO_3$	0.004
$Ar + O_2 + H_2O$	80	$CdTe_2O_5$	0.022
9 mTorr $CdCl_2$ + Ar+ O_2	<1	CdO, $CdTeO_3$	0.007
9 mTorr $CdCl_2$ + Ar + O_2 + H_2O	80	$CdTe_2O_5$	>0.050

By raising the sample treatment temperature, reducing the $CdCl_2$ vapor concentration, by reduction of source temperature, and reducing the oxygen concentration in the ambient mixture, we achieved samples which yielded no detectable surface oxide phases for treatments of 30 sec and 1 minute: GIXRD analysis of samples treated in $CdCl_2$:Ar:O_2 vapor for 1-2 minutes at 480°C and at 500°C for 30 seconds revealed no detectable oxides. In such cases, the aniline etch step can be completely eliminated while maintaining device performance (Table IV). The samples all exhibited identical current densities but with slightly lower V_{OC} and FF for cells treated for 30 seconds.

Table IV. Best cell results for samples processed from a single VT plate with baseline (2 minute) $CdCl_2$ treatment time and reduced (30 second) treatment time.

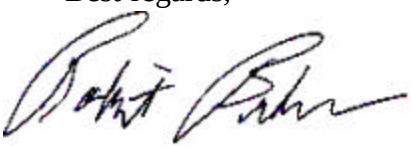
Run Number	$CdCl_2$ Step	Etch Step	V_{OC} (mV)	J_{SC} mA/cm^2	FF (%)	Eff (%)
240.3	2 min 480C	2 min	782	24.8	68.8	13.3
240.4a	30 sec 500C	1 min	744	24.8	62.2	11.5
240.4b	30 sec 500C	none	741	24.8	66.8	12.3

Vapor transport depositions with reduced CdTe thickness have been carried out to provide plates to use post-deposition optimization experiments. Continuous films with thickness from 1 to 3 microns have been deposited onto CdS coated Ga_2O_3/TEC15 superstrates. Simple approaches for mitigating the effects of pinholes in CdTe are being developed to allow large area cells to be fabricated having comparable performance to small area cells. The pinhole mitigation treatment (PMT) relies on preferential formation of polymer insulators in pinhole regions. Table V shows cell yield and performance data for samples with 3 micron thick CdTe deposited onto non-optimal CdS films; these films had been rejected for baseline processing due to the presence of a surfacial powdery CdS residue that often leads to pinholes in the CdTe film. The plates selected had >1 micron wide pinholes in the CdTe film at an area density exceeding 100 per cm^2. Sample 195.4 was processed without the PMT and only yielded one cell out of eight that was not shorted. An adjacent piece, VT195.2, was processed with the PMT and yielded six out of eight with similar performance to the only live cell on VT195.4. Finally, an entire plate, VT268, received the PMT and one 8 cm L x 0.9 cm W cell was fabricated, with comparable V_{OC} to the small area cells made on the VT195 samples. The current and FF are low on this sample due to series loss, from non-optimized point contacts. The V_{OC} results, on materials with known mechanical deficiencies, demonstrate the efficacy of the PMT process for improving device yield in cases where marginal lateral film density has been obtained.

Table V. Yield and best cell for VT CdTe/CdS processed with and without pinhole mitigation technique

Run Number	PMT ?	Cell Area (cm^2)	Cell Yield	V_{OC} (mV)	J_{SC} mA/cm^2	FF (%)	Eff (%)
195.4	N	0.4	1/8	778	23.7	58.7	10.8
195.2	Y	0.4	6/8	778	24.0	50.0	9.4
268.1	Y	7.0	1/1	781	7.1	28.3	1.6

Best regards,



Robert W. Birkmire
Director

1 B.E. McCandless, M.G. Engelmann, R.W. Birkmire, "Modeling X-Ray Diffraction Line Profiles of CdS/CdTe Thin Films," Journal of Applied Physics, (2000), 89 (2) 988-995.

/eak

cc: Paula Newton, IEC
Susan Tompkins, OVPR, UD
Carolyn Lopez, NREL